Generalized SVPWM Algorithm for Two Legged Three Phase Multilevel Inverter

Devisree Sasi¹, Jisha Kuruvilla P¹, Anish Gopinath²

¹Department of Electrical and Electronics Engineering, Mar Athanasius College of Engineering, Kerala, India ²Scientist-SD, CECD, VSSC, ISRO, Kerala, India

Article Info	ABSTRACT
Article history:	This paper establishes the inherent fractal structure in the space vector
D : 11 10 0010	representation of two legged three phase multilevel inverters. The established

Received Jun 12, 2013 Revised Aug 8, 2013 Accepted Aug 26, 2013

Keyword:

Four switch three phase inverter (FSTPI) topology Fractals Space vector pulse width modulation (SVPWM) Two legged multilevel inverters This paper establishes the inherent fractal structure in the space vector representation of two legged three phase multilevel inverters. The established fractal structure is utilized to propose a generalized algorithm for space vector PWM generation for two legged multilevel inverters. The voltage space vectors of higher level inverters can be generated from the voltage space vectors of equivalent 2-level inverter. The proposed algorithm can be easily extended to n-level inverters without any computational complexity and it doesn't use any look up table for sector identification. The paper explains the proposed method for 5-level inverter and simulation results are presented for 2-level, 3-level and 5-level configurations in MATLAB/SIMULINK.

Copyright © 2013 Institute of Advanced Engineering and Science. All rights reserved.

Corresponding Author:

Devisree Sasi, Department of Electrical and Electronics Engineering, Mar Athanasius College of Engineering, Kerala, India. Email: devisreesasi@gmail.com

1. INTRODUCTION

In recent years multilevel inverter technology has emerged as a very important alternative in the area of high power applications due to high Voltage-Ampere rating and better harmonic rejection capabilities. In comparison to 2-level inverter, multilevel inverter generates sinusoids from multiple levels of dc voltage with lesser harmonic distortion. As the number of levels increases, the synthesized output waveform adds more steps, producing a staircase wave which approaches the sinusoidal wave and the harmonic content of output voltage waveform decreases significantly [1], [2]. The requirement of increased number of semiconductor switches is the major disadvantage of multilevel inverters due to increased switching losses, electromagnetic interference (EMI) and also the overall system become more complex and expensive. So in many critical applications multilevel inverter with reduced number of switches drawing significant research attention. A conventional three phase inverter has three legs with a pair of complementary power switches per leg (Six Switch Three Phase Inverter-SSTPI). The four switch inverter topology (Four Switch Three Phase Inverter-FSTPI) with two legs and four switches is one of the techniques to reduce the number of switches in the inverter [3]. In comparison to SSTPI, the main features of FSTPI are reduced number of switches, lower switching losses, reduced number of driver circuits and less expensive.

Various pulse width modulation (PWM) techniques are utilized for the efficient operation of multilevel inverters [4]-[6]. Most commonly used PWM technique is Sine-Triangle PWM (SPWM) in which PWM signals are generated by comparing the sine wave with a number of level shifted triangular carrier signals [7]. With the developments of digital signal processors the Space Vector PWM (SVPWM) technique become most popular and efficient method for inverters and it synthesize the reference voltage space vector

by switching three nearest voltage space vectors [8]-[10]. SVPWM technique is the best choice for the multilevel inverters due to its inherent advantages of better dc voltage utilization, reduced switching losses, lower harmonic distortion and easier implementation. There has been lots of works in the area of SVPWM for FSTPI [11]-[14], but its extension to multilevel inverters is yet to be explored.

The paper explores a simple method to extent the SVPWM for FSTPI to multilevel configurations. The paper begins with the observation that the space vector representation of two legged multilevel inverters has an inherent fractal structure. The paper also found that the voltage space vectors of higher level inverter can be generated from the voltage space vectors of equivalent 2-level inverter using simple arithmetic operations. The observation in the paper is utilized to prepare a simple and generalized algorithm for two legged multilevel inverters without any computational complexity. The proposed method explained the sector identification for the implementation of SVPWM without any look up table. Finally the proposed algorithm is simulated in MATLAB/SIMULINK for 2-level, 3-level and 5-level configurations.

2. SPACE VECTOR REPRESENTATION OF TWO LEGGED MULTILEVEL INVERTERS

In SVPWM scheme the reference space vector is synthesized by switching three nearest voltage space vectors. The reference space vector is obtained by combining the effect of three instantaneous reference phase voltages. The triangle formed by three voltage space vectors as vertices is known as a sector. Figure 1 shows the space vector representation of conventional 2-level three phase inverter (SSTPI. It has six sectors numbered S_1 - S_6 as in Figure 1(a). The voltage space vector representation of two legged 2-level three phase inverter has four inverter voltage vectors located at the vertices of the parallelogram which be divided into two equilateral triangles (sectors) numbered as S_1 and S_2 as in Figure 1(b). Sector 1 is formed by the voltage vectors located at A_{01} , A_{02} and A_{03} and sector 2 is formed by the vectors located at A_{01} , A_{03} and A_{04} . Two legged 2-level inverter configuration referred as four switch three phase inverter topology (FSTPI) in literature. It may be noted from Figure 1 that compared to SSTPI, FSTPI has only two triangles for encompassing the reference voltage space vector. The advantage of lesser triangles further simplifies the SVPWM generation for two legged higher level inverter configurations.



Figure 1. Space Vector Representation of (a) SSTPI (b) FSTPI



Figure 2. Space Vector Representation of Two Legged 3-level Inverter

IJPEDS

Figure 2 shows the voltage space vector locations of two legged 3-level inverter. It may be noted from figure 1(b) and figure 2 that space vector representation of 3-level inverter has five additional voltage space vectors compared to equivalent 2-level inverter configuration and are located at A_{11} , A_{12} , A_{13} , A_{14} and A_{00} . These five additional voltage vectors of 3-level inverter are located at the midpoints of the each side of the sectors of the equivalent 2-level inverter. A_{11} is located at the midpoint of the vector locations A_{01} and A_{02} . The space vector locations A_{12} , A_{13} , A_{14} and A_{00} are also located similarly. The five additional voltage space vectors increases the total number of sectors of 3-level inverter to 8. Thus the sectors of 3-level inverter can be generated from sectors of 2-level inverter by dividing each sectors of 2-level inverter into four smaller triangular sectors.



Figure 3. Generating Sectors of Two Legged, 3-level Inverter from Sectors of Equivalent 2-level Inverter

Figure 3 shows the generation of space vector representation of two legged 3-level inverter from the space vector representation of equivalent 2-level inverter. The space vector representation of two legged 2-level inverter is shown in Figure 3(a). The midpoints of each side of two sectors of 2-level inverter are computed and are shown as solid dots in Figure 3(b). The joining of the three midpoints of the sides of the sectors of 2-level inverter will result the space vector representation of 3-level inverter as in Figure 3(c). In the same manner the voltage space vector representation of 5-level inverter is generated from the equivalent 3-level inverter. Compared to 3-level configuration, in the case of 5-level inverter configuration sixteen additional voltage vectors are present and are located at the midpoints of the sides of the sectors of equivalent 3-level inverter. The sixteen additional voltage vectors results 32 sectors in the space vector representation of 5-level inverter. The process gets repeated as the number of levels increases.

The voltage space vector representation of any level inverter can be generated from the space vector representation of equivalent 2-level inverter, whereas the sectors of 2-level inverter is progressively divided and subdivided. According to fractal theory, any basic structure continuously decomposes in to smaller structures which again look very similar to the whole as well as to its basic structure is said to have fractal structure [15]. From that point of view, the voltage space vector representation of two legged multilevel inverter has an inherent fractal structure with triangle as basic structure which is transformed by further dividing itself in to smaller triangles. The process of generation of triangle by joining the midpoints of the triangle is known as Sierpinski triangle generation in fractal theory [15].



Figure 4. (a) Voltage space vectors of two legged 5-level inverter (b) Switching states of two legged 5-level inverter

Due to the fractal structure the voltage space vector representation of 2-level inverter grows to the higher level inverters by repeated division of each sector. The sectors of higher level inverter can therefore be generated by repeated triangularization algorithm [10]. This observation is utilized to prepare a simple and generalized algorithm for the generation of SVPWM signals for two legged multilevel inverters. Switching vectors and corresponding switching states of higher level inverters are also be generated from equivalent 2-level inverter by using repeated triangularization algorithm [10]. The number of applications of triangularization algorithm depends on the levels of the inverter. The space vector representation of two legged 5-level inverter and inverter switching states are shown in Figure 4.

The number of sectors of two legged inverter for 2-level, 3-level, 5-level and 9-level configurations are 2, 8, 32 and 128 respectively. Generalizing the number of sectors, s, of two legged n-level inverter is:

$$S = 2 \times (n-1)^2 \tag{1}$$

The number of sectors of conventional three phase n-level inverter is:

$$s = 6 \times (n-1)^2 \tag{2}$$

It may be noted that the number of sectors of two legged n-level inverter is only one third of the number of conventional inverters. The reduction in the number of sectors simplifies the generation of SVPWM for two legged multilevel inverters.

3. PROPOSED SVPWM ALGORITHM FOR TWO LEGGED MULTILEVEL INVERTERS

In SVPWM scheme the space vector concept utilized for computing the duty cycle of the semiconductor switches in the inverter. SVPWM technique involves synthesizing the reference voltage space vector by switching three nearest voltage space vectors. The implementation of SVPWM using proposed algorithm involves the following steps: (i) Identification of sector which encloses the tip of the reference space vector (ii) Determination of inverter switching vectors and corresponding switching states (iii) Computation of duration of the three switching voltage vectors.

3.1. Sector Identification

Sector identification finds out the sector in which the tip of the instantaneous reference space vector lies. The voltage space vectors located at the vertices of the identified sector are used to synthesize the reference space vector. The reference space vector is obtained from the combined effect of three instantaneous reference phase voltages. The reference space vector is represented in (α , β) plane. From the three reference phase voltages V_a, V_b, and V_c the α and β coordinates of the reference space vector can be obtained as:

$$V_{\alpha} = \frac{3}{2} V_{a}$$

$$V_{\beta} = \frac{\sqrt{3}}{2} \left(V_{b} - V_{c} \right)$$
(3)



Figure 5. The Position of Instantaneous Reference Space Vector OP in Two Legged 5-level Inverter

In order to illustrate the sector identification in the proposed method, consider the position of instantaneous reference space vector OP as shown in Figure 5. The illustration of sector identification used in the proposed work is shown in Figure 6. In the proposed method, sector identification begins with determining the sector enclosing the reference space vector from among the two regions of an equivalent 2-

level inverter. The inverter switching vectors and corresponding switching states for an equivalent 2-level inverter is shown in Figure 6(a). The first step is computing the centroids of the two sectors of equivalent 2-level inverter. Since the sectors are equilateral triangles the centroid of each sector is computed by taking the average of the coordinates of the three vertices. The distance of the tip of the reference space vector from each of these centroids is determined and the triangle with centroid closest to the tip of the reference space vector is the sector to be identified.



Figure 6. Illustration of the Proposed Sector Identification for a 5-level Two Legged Inverter

In this case $\Delta A_{01}A_{02}A_{03}$ is the triangular sector in which tip of the reference space vector lies as shown in Figure 6(a). Triangularization algorithm is applied in $\Delta A_{01}A_{02}A_{03}$ which results three additional vectors A_{11} , A_{12} and A_{00} which are the midpoints of each sides of the $\Delta A_{01}A_{02}A_{03}$ of equivalent 2-level inverter. Joining these midpoints A_{11} , A_{12} and A_{00} divide the $\Delta A_{01}A_{02}A_{03}$ into four equilateral triangles as in Figure 6(b). The voltage vectors and switching states of the three additional vectors A_{11} , A_{12} and A_{00} are also computed using the triangularization algorithm and are obtained as in Figure 6(b). The centroids of newly created four triangles are computed. The location of the tip of the reference voltage space vector from among these four sectors is found by determining the sector whose centroid is closest to the tip of the reference voltage space vector. Thus the triangular sector which encloses the tip of the reference space vector is identified as $\Delta A_{00}A_{11}A_{12}$.

For 5-level inverter the number of applications of triangularization algorithm is two [10] and hence it has to be applied once more. The application of triangularization algorithm to $\Delta A_{00}A_{11}A_{12}$ will further generate three new voltage space vectors A_{21} , A_{22} and A_{23} and by joining these vectors $\Delta A_{00}A_{11}A_{12}$ will further divided into four equilateral triangles as shown in Figure 6(c). The application of triangularization algorithm also generate the voltage space vectors and switching states of the newly created three voltage space vectors A_{21} , A_{22} and A_{23} . The centroid of the four sectors within $\Delta A_{00}A_{11}A_{12}$ is computed and triangle with centroid closest to the tip of the reference space vector is determined. From among the four newly created sectors, $\Delta A_{21}A_{22}A_{23}$ is identified as the sector in which the tip of the reference space vector lies. This is the procedure for the sector identification and for higher level inverters the process repeated. Thus in the proposed method the identification of sector is done without using any look up tables. The switching states corresponding to the voltage vectors located at the vertices of the identified sector are also generated simultaneously.

3.2. Computation of Switching Voltage Vector Duration

The determination of the switching voltage vectors and corresponding switching states of the identified sectors are explained in the previous section. The next step in the generation of SVPWM involves computing the duration for which the voltage space vectors at the vertices of the identified sector are to be switched. The duration of the switching voltage vectors are determined using the volt-sec balancing principle [8]. Switching time durations of the three voltage space vectors are dented as T_0 , T_1 and T_2 . According to volt-sec balancing principle, the equations of switching time durations (T_1 and T_2) of the voltage space vectors for two legged 3-level inverter are given in Table 1. The sampling time period, T_S , is equal to the sum of T_0 , T_1 and T_2 . Thus the equation for T_0 is obtained as:

$$T_0 = T_s - T_1 - T_2 \tag{4}$$

The equations of gating signal time for phase A and phase B (T_{ga} and T_{gb}) for two legged 3-level inverter are also given in Table 1.

Table 1. Switching Time Equations for 3-level Inverter					
Sector	T ₁	T ₂	T _{ga}	Tgb	
\mathbf{S}_1	$\left[2V_{\alpha}-\frac{2}{\sqrt{3}}V_{\beta}\right]T_{s}$	$\frac{4}{\sqrt{3}}V_{\beta}T_{s}$	$T_1 + T_2$	T_2	
S_2	$\left[2V_{\alpha}-\frac{2}{\sqrt{3}}V_{\beta}-1\right]T_{s}$	$\left[\frac{4}{\sqrt{3}}V_{\beta}+1\right]T_{s}$	$T_1 + T_2$	T_2	
\mathbf{S}_3	$\left[-2V_{\alpha}+\frac{2}{\sqrt{3}}V_{\beta}+1\right]T_{s}$	$\left[2V_{\alpha}+\frac{2}{\sqrt{3}}V_{\beta}\right]T_{s}$	T_2	$T_1 + T_2$	
\mathbf{S}_4	$\left[2V_{\alpha}-\frac{2}{\sqrt{3}}V_{\beta}\right]T_{s}$	$\left[\frac{4}{\sqrt{3}}V_{\beta}T_{s}+1\right]$	$T_1 + T_2$	T_2	
S_5	$\left[-2V_{\alpha}+\frac{2}{\sqrt{3}}V_{\beta}\right]T_{s}$	$\left[2V_{\alpha} + \frac{2}{\sqrt{3}}V_{\beta} + 1\right]T_{s}$	T_2	$T_1 + T_2$	
S_6	$\left[-2V_{\alpha}+\frac{2}{\sqrt{3}}V_{\beta}-1\right]T_{s}$	$\left[2V_{\alpha} + \frac{2}{\sqrt{3}}V_{\beta} + 1\right]T_{s}$	T_2	$T_1 + T_2$	
\mathbf{S}_7	$\left[2V_{\alpha}-\frac{2}{\sqrt{3}}V_{\beta}+1\right]T_{s}$	$\frac{4}{\sqrt{3}}V_{\beta}T_{s}$	$T_1 + T_2$	T_2	
S_8	$\left[-2V_{\alpha}+\frac{2}{\sqrt{3}}V_{\beta}\right]T_{s}$	$\left[2V_{\alpha}+\frac{2}{\sqrt{3}}V_{\beta}\right]T_{s}$	T_2	$T_1 + T_2$	

4. SIMULATION RESULTS

The proposed algorithm has been simulated in MATLAB/SIMULINK for two legged three phase inverter fed Permanent Magnet Synchronous Motor (PMSM) drive with a DC link voltage of 400V. Figure 7 presents the simulation results for 2-level, 3-level and 5-level configurations with phase C clamped to 200V. PMSM parameters are given in Appendix. Figure 7(a) represents the gating signal waveform for 2-level, 3-level and 5-level configurations. The gating signal waveforms for 3-level inverter are obtained from the equations given in Table 1. Figure 7(b) shows the pole voltage waveforms corresponding to 400V operation for 2-level, 3-level and 5-level configurations. For two legged 2-level configurations the inverter switches between 0V and 400V. For 3-level operation the inverter switches between the levels of 0V, 200V and 400V. The levels of pole voltage for 5-level operations are 0V, 100V, 200V, 300V and 400V as in Figure 7(b). PMSM phase voltages and current waveforms for 2-level, 3-level and 5-level configurations are given in Figure 7(c) and Figure 7(d) respectively.





Figure 7. Simulation Results of Two Legged Inverters (2-level, 3-level and 5-level configuration)

5. CONCLUSION

The paper established that the voltage space vector representation of two legged multilevel inverters has an inherent fractal structure and proposes a simple and generalized algorithm for SVPWM generation for two legged multilevel inverters using this fractal structure. The paper also observe that the voltage space vectors of higher level inverters can be generated from the voltage space vectors of 2-level inverter using simple arithmetic operations. The sector identification in the proposed algorithm is also simple and it doesn't use any look up tables. The proposed method can be easily extended to n-level inverters. The simulation results are presented in MATLAB/SIMULINK for two legged inverters in order to validate the proposed algorithm.

REFERENCES

- [1] JS Lai, FZ Peng. Multilevel converters–A new breed of power converters. *IEEE Transactions on Industrial Applications*. 1996; 32: 509–517.
- [2] Jose Rodriguez, Jih-Sheng Lai, Fang Zheng Peng. Multilevel Inverters: A Survey of Topologies, Controls and Applications. *IEEE Transactions on Industrial Electronics*. 2002; 49(4): 724-738.
- [3] HW van der Broeck, JD van Wyk. A comparative investigation of a three-phase induction machine drive with a component minimized voltage-fed inverter under different control options. *IEEE Transactions on Industrial Applications*. 1984; IA-20(2): 309–320.
- [4] J Holtz. Pulse width modulation: A survey. IEEE Transactions on Industrial Electronics. 1992; 39(5): 410-420.
- [5] K Zhou, D Wang. Relationship between space-vector modulation and three-phase carrier-based PWM: A comprehensive analysis. *IEEE Transactions on Industrial Electronics*. 2002; 49(1): 186–196.
- [6] W Yao, H Hu, Z Lu. Comparisons of space-vector modulation and carrier based modulation of multilevel inverter. *IEEE Transactions on Power Electronics*. 2008; 23(1): 45–51.
- [7] BP McGrath, DG Holmes. Multi carrier PWM strategies for multilevel inverters. *IEEE Transactions on Industrial Electronics*. 2002; 49(4): 858–867.
- [8] HWVD Brocker, HC Skudenly, GV Stanke. Analysis and realization of a pulse width modulator based on the voltage space vectors. *IEEE Transactions on Industrial Applications*. 1988; 24(1): 142-149.
- [9] Aneesh Mohamed AS, Anish Gopinath, MR Baiju. A simple space vector PWM generation scheme for any general n-level inverter. *IEEE Transactions on Industrial Electronics*. 2009; 56(5): 1649-1656.
- [10] Anish Gopinath, Aneesh Mohamed AS, MR Baiju. Fractal based space vector PWM for multilevel inverters A novel approach. *IEEE Transactions on Industrial Electronics*. 2009; 56(4): 1230–1237.
- [11] CB Jacobina, ERC da Silva, AMN Lima, RLA Ribeiro. Vector and scalar control of a four switch three phase inverter. *Proc. IEEE-IAS Annual Meeting*. 1995; 2422–2429.
- [12] MBR Corrêa, CB Jacobina, ERC Silva, AMN Lima. A General PWM Strategy for Four-Switch three phase inverter. *IEEE Transactions on Power Electronics*. 2006; 21(6): 1618-1627.
- [13] Frede Blaabjerg, Sigurdur Freysson, H Henrik Hansen, S Hansen. A new optimized space vector modulation strategy for a component minimized voltage source inverter. *IEEE Transactions on Power Electronics*. 1997; 12(4): 704-714.

- [14] PQ Dzung, LM Phuong, PQ Vinh, NM Hoang, TC Binh. New Space Vector Control Approach for Four Switch Three Phase Inverter (FSTPI). International Conference on Power Electronics and Drive Systems- PEDS. Bangkok, Thailand. 2007.
- [15] HO Peitgen, H Jurgens, D Saupe. Chaos and Fractals—New Frontiers of Science, 2nd ed. New York: Springer-Verlag, 2004.

APPENDIX Parameters of PMSM			
Stator resistance	0.7Ω		
Stator inductance	2.72mH		
Back-emf constant	0.5128V/rad/sec		
Moment of inertia	0.0002kgm ²		
Damping coefficient	0.002Nms/rad		

BIOGRAPHIES OF AUTHORS



Devisree Sasi received the B.Tech. degree in Electrical and Electronics Engineering from Government Engineering College, Idukki, Kerala, India in 2010. Currently she is pursuing her M.Tech in Power Electronics in Mar Athanasius College of Engineering, Kothamangalam, Kerala, India.

Email: devisreesasi@gmail.com



Jisha Kuruvilla P received B.Tech. degree in Electrical and Electronics Engineering from LBS College of Engineering, Kasargode, Kerala, India in 2001 and the M.Tech degree in Power Electronics and Drives from PSG Tech., Coimbatore, Tamil Nadu, India in 2011. She is currently working as an Assistant Professor in the Department of Electrical and Electronics Engineering in Mar Athanasius College of Engineering, Kerala, India. Email: Jishakuruvillamace@gmail.com



Anish Gopinath completed B.Tech and M.Tech in Applied Electronics and Instrumentation from the College of Engineering, Thiruvananthapuram, under the University of Kerala in 2004 and 2007 respectively. Since then, working in the Control Electronics and Checkout Group of Avionics, Vikram Sarabhai Space Centre ISRO Thiruvananthapuram. Areas of interests are Space Vector PWM, Multilevel Inverters, Multi phase Motors, BLDC motor drives, High power motor drives for aerospace application. Reviewer of IEEE Industrial Electronics Society for IEEE Transactions on Industrial Informatics. Email: gopinathanish@gmail.com